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10A.1
Electronic Packaging Technologies

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Electronic packaging is the art and science of connecting circuitry to reliably perform some desired function in some application environment. Packaging also provides ease of handling and protection for assembly operations. This chapter defines chip, or die-level, and assembly-level packaging, with an emphasis on recent technologies. The relative advantages of each technology will be discussed in relation to performance, cost, reliability, and manufacturability. Extensive details on electronic packaging can be found in the references.[1–6]

10A.1.1   Packaging the Die

A semiconductor device, also known as a *die* or *chip*, is fragile and must be packaged for protection and for interfacing with the outside world. The chip package provides an electrical interconnection to the assembly, module, or display and protects the chip in the manufacturing and application environments. A number of different materials can be used in the die package, including ceramics, plastics, and metals. Single-chip, three-dimensional, and multichip module (MCM) packages are some of the packaging formats. Interconnection is the process and technique of making electrical connections between the bond pads of the chip and a leadframe, substrate, or even another chip.

Plastic Die Package

Plastic packages are very popular in commercial applications because of their low cost and small size compared to ceramic packages. The cost of plastic packages is typically one half to one tenth the cost of comparable ceramic or metal packages. More than 98% of all integrated circuits were packaged in plastic in 1992. In a plastic package, the chip is encapsulated by a polymer, usually referred to as the *encapsulant*. An encapsulant is generally an electrically insulating material formulation that protects an electronic device and die-leadframe assembly from the adverse effects of handling, storage, and operation.
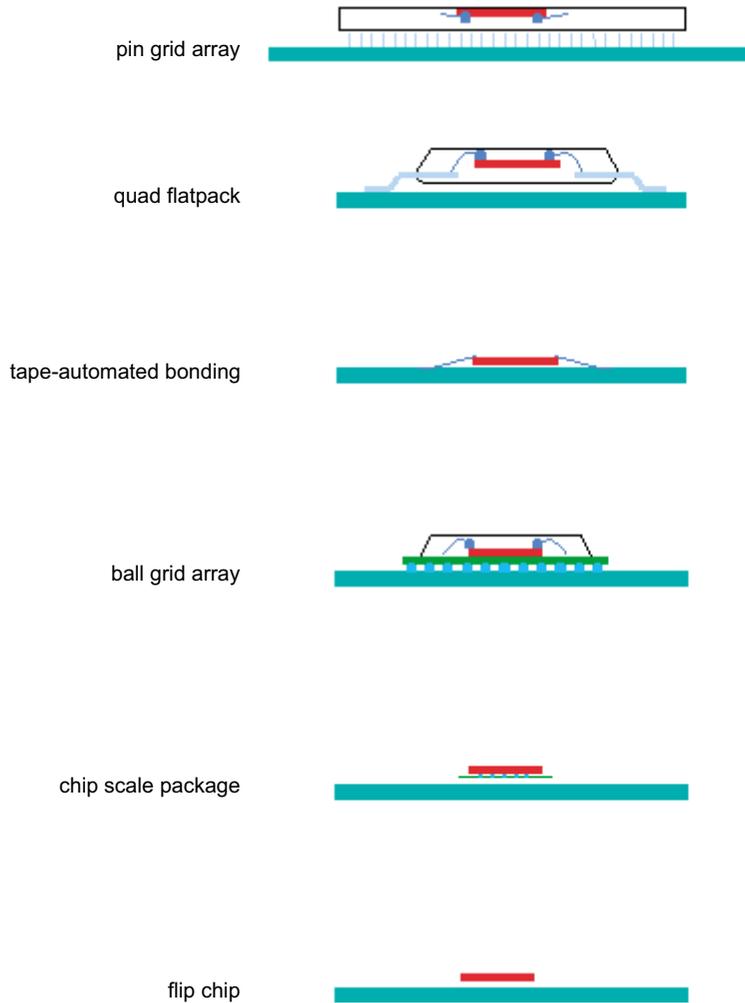
FIGURE 10A.1.1 Shrinking size of packaging.

Figure 10A.1.1 depicts the evolution of packaging shrinkage through the last three decades. Packaging size is being pressed by the shrinking feature size (approximately 15% per year) of CMOS integrated circuits. Package lead styles have changed dramatically from the 1970s when the dual in-line package (DIP) and pin grid array dominated the semiconductor industry. Even today, the DIP retains a sizable share of the market in which low-cost, rugged packaging meets the application need. Generally, there are at least three major lead types, with numerous variations of each: the through-hole, the surface-mount (J- or gull-lead), and the solder ball. The through-hole and leaded surface-mount packages usually have a leadframe to which the die is mounted. The plastic solder ball packages typically employ organic substrates that redistribute the die inputs-outputs (I/O) to an array or perimeter pattern of solder balls. (Substrate technologies are addressed in Section 10A.1.2.)

In the late 1980s, 1.27-mm pitch, surface-mount technology became prominent. As device complexity increased, the I/O count also increased. To keep electrical performance and package sizes reasonable, the lead pitch decreased, and fine-pitch leaded devices (lead pitch of less than or equal to 0.65 mm) were introduced.

Array packaging was first introduced in the mid-1970s with ceramic pin grid array packages. Surface-mount array packages evolved to plastic ball grid array (PBGA) and chip-scale packages (CSP). Solder

TABLE 10A.1.1 Typical Coplanarity Requirements for SMT Components[7]

Component	Pitch (mm)	Coplanarity Requirement (mm)
Leaded SMT	—	0.10
PBGA	1.27 –1.5	0.20
	1.0	0.15
	<1.0	0.08
CBGA	—	0.15
CSP	—	0.08

From Hwang, J.S., BGA and CSP solder spheres, *Surface Mount Technology,* April, p. 18, 1999. © 1999 by IHS Publishing Group (www.smtmag.com). With permission.

spheres — usually composed of 63% tin and 37% lead, 62/36/2 (% silver), or high-temperature 10/90 — form the connection between the package and the board.

The chip-scale package is typically defined as being not more than 20% larger than the die. The CSP interposer buffers the final assembly from die-shrink redesign. The interposer can be organic substrate, tape-automated bonded (TAB), or ceramic substrate. The interposer can also act as a stress buffer between the low thermal expansion of the semiconductor die and the higher expansion of the substrate. Tessera (San Jose, CA) adds a patented elastomer between the die and the interposer to further buffer the solder balls. While the majority of CSP used today have solder-ball interconnects, there are non-solder-ball variations that meet the CSP definition, such as the small-outline, no-lead (SON) and bottom-leaded plastic packages (BLP).

The coplanarity of surface-mount parts is an important mechanical parameter in assembly. Non-planar parts can lead to poor assembly yields (voids, electrical opens) and unreliable connections (misregistration). Table 10A.1.1 outlines typical coplanarity requirements.

Encapsulation techniques include molding, potting, glob-topping, and conformal coating, but the majority of encapsulated packages use the molding process. The molding compound is a proprietary multicomponent mixture of an encapsulating resin with various types of additives. The principal active and passive (inert) components in a molding compound include curing agents or hardeners, accelerators, inert fillers, coupling agents, flame retardants, stress-relief additives, coloring agents, and mold-release agents. Molding compounds have moved steadily toward all-epoxy systems.

Thermosetting encapsulation compounds are based on epoxy resins. In electrical and electronic applications, three types of epoxy resins are commonly used: the diglycidyl ethers of bisphenol A (DGEBA) or bisphenol F (DGEBF), the phenolic and cresol novolacs, and the cycloaliphatic epoxides. Novolac-based epoxies are supplied as molding bricks (preforms) that are ready for use in transfer-molding machines to produce single-in-line packages, dual-in-line packages, plastic leaded chip carriers, quad flatpacks, various types of small-outline integrated circuits (SOIC), and ball grid array packages.

Pin grid array carriers, some ball grid array packages, and carriers with metal cans frequently use multicomponent liquid epoxies or preforms. Flip chips mounted on organic substrates also use liquid epoxy underfills to protect the die surface environmentally as well as to provide stress relief to the solder balls. Polyurethanes, polyamides, and polyesters are used to encase modules and hybrids intended for use under low-temperature and high-humidity conditions. Modified polyimide encapsulants have the advantages of thermal and moisture stability, low coefficient of thermal expansion, and high material purity. Thermoplastics are rarely used because they generally require processing conditions of unacceptably high temperature and pressure, are low-purity materials, and can induce high moisture-induced stresses.

Several molding techniques (Table 10A.1.2) are available for the manufacture of plastic cases. The most widely used manufacturing process is the transfer molding process, used for molding thermosetting polymers. These polymers are plastic or fluid at low temperatures but, when heated, react irreversibly to

TABLE 10A.1.2 Comparison of Molding Processes

Molding type	Advantages	Disadvantages
Transfer molding	Multiple cavities, high yield Relative material savings Short cycle time Low tool maintenance costs	High molding pressure High viscosity Restricted to the packaging of leadframes
Injection molding	Good surface finish Good dimensional control	Poor material availability
Reaction-injection molding	Energy efficiency Low mold pressure Good wetting of chip surface Adaptability to TAB	Few resin systems available for electronic packaging Requires good mixing

form a cross-linked network no longer capable of being melted. Other processes include the injection molding process and the reaction-injection molding process.

Hermetic (Metal and Ceramic) Packages

Hermetic packages have been used predominantly for military and government applications because of their perceived reliability advantage over plastic packages. They have also been employed in some high-power applications when heat must be dissipated from the device. Metal packages are typically used for small integrated circuits with a low lead count and in applications that require electromagnetic shielding.

Both metal and ceramic packages can be made nearly impervious to moisture when hermetically sealed. A package is classified as hermetic if it has a minimal leak rate (the rate at which gases can diffuse into or out of the package). Typical acceptable helium leak rates depend on the package size and helium pressure in the package. Some metal packages (e.g., Olin Metal quad flatpacks) are sealed using epoxies and, therefore, are not hermetic.

Several major semiconductor companies (Intel, Motorola, and AMD) have announced their exit from military markets, and the availability of these packages is shrinking dramatically. Plastic components are finding their way into many applications that had once been dominated by hermetic packages.

Interconnection Technologies at the First Level of Packaging

The major interconnection technologies at the first level of packaging are wirebonding, flip chip, and TAB. Wirebonding, the mainstay of the microelectronics industry, still accounts for more than 98% of all semiconductor interconnections. Invented more than 30 years ago, flip chip was once available only to large, vertically integrated companies. Now, contract sources of wafer bumping are available, making flip chip one of the fastest growing interconnect methods. Tape-automated bonding (TAB) techniques are mature, although they are utilized only in limited, specialized applications because of high tooling costs. Chip stacking or three-dimensional (3-D) interconnection is typically used in systems where size, weight, and speed are critical. Comparisons of these technologies are provided in Tables 10A.1.3 and 10A.1.4.

Wirebond Interconnects

Wirebond interconnects are formed by metallurgically bonding a small-diameter wire from the semiconductor device to the leadframe, substrate, or other semiconductor. The wirebond forms a low-resistance path for signal propagation. Typical wire materials include aluminum, gold, and copper. Gold is usually bonded by thermocompression, while aluminum is usually bonded ultrasonically.

Common materials for pads on bondable surfaces include aluminum, gold, silver, nickel, and copper. Aluminum and gold are the most frequently used bondpad materials. Silver has been used as a bondable plating material on leadframes and as a bondable thick-film metallization in alloy form with platinum

TABLE 10A.1.3 Comparison of Interconnect Technologies

Attribute	Wirebonding	TAB	Flip TAB	Flip Chip	High-Density Interconnects
Minimum (and typical) I/O pitch (μm)	100 (150)	50 (100)	50 (100)	125 (250)	25/1 (50/2)
Maximum I/O range	256–500	400–700	400–700	>800	>1000
Lead inductance (nH)	1–2	1	0.1	0.05–0.1	<0.05
Mutual inductance between leads (pH)	100	5	5	1	<1
Typical effective diameter (μm)	25	50	50	125	N/A
Typical length (mm)	1	1	0.25	0.1	N/A
Connection technique	Perimeter; array area is difficult but possible, using multi-height loops	Perimeter; array area is moderately difficult but possible, using multilayer tape	Perimeter; array area is moderately difficult	Perimeter and array area	Perimeter and array area
Packaging efficiency	Medium	Medium	Medium-high	High	High
Pretestability in fine pitch	Difficult with available instrumentation	Good	Good	Difficult with available instrumentation	Difficult with available instrumentation
Ability to rework	Difficult	Fair	Good	Good	Good
Loop control	Fair	Good	Good	Good	Good
Flexibility of the manufacturing process	Excellent	Fair (gang bonding); good (single-point bonding)	Fair (gang bonding); good (single-point bonding)	Good	Good
Dominant failure mechanisms	Fatigue, bond-pad corrosion	Lead fatigue, interdiffusion	Lead fatigue, interdiffusion	Fatigue, intermetallics	Electromigration, corrosion
Heat dissipation	Good (die bonded to substrate)	Good (die bonded to substrate)	Poor, but excellent if heat sink attached to back side	Poor, but excellent if heat sink attached to back side	Good (die bonded to substrate)
Die availability	Excellent	Fair	Fair	Poor	Excellent
Tool availability	Excellent	Fair	Fair	Fair	Fair
Technology maturity	Excellent	Good	Good	Good	Fair
Market share	98%	<2%	<1%	<1%	<1%
Cost	Low	Medium	Medium	High (potentially low)	High (potentially low)

TABLE A10.1.4 Relative Advantages of Interconnect Technologies

	Advantages	Disadvantages
Wirebond	Low resistance interconnects Low capital investment Mature technology Highly stable manufacturing process	Potential for cross-talk High lead inductance Use of costly, precious metal wire Low interconnect density Limited chip size
Flip chip	Self-alignment during die joining Automatic die placement and testing Low lead inductance Less need for precious metals Simultaneous bonding	Potential for solder fatigue Thermal dissipation concerns
TAB	Lightweight packaging Small size/high I/O-count Simultaneous bonding	High capital investment
HDI	Power and signal distribution High frequency performance High clock-rate performance High wiring densities High device-to-substrate area ratio	Process not fully mature High cost of deposited HDI
3-D	Increased package density Better board utilization Increased electrical performance Shorter interchip connections Lower system power	Potential for cross-talk Thermal dissipation concerns Poor yields Process not fully mature

or palladium.[8] Nickel has been widely used as a substitute for gold in power devices. In addition, nickel or chromium serve as barrier layers to avoid unwanted intermetallic compounds and to facilitate adhesion.

Thermocompression and thermosonic bonds are typically used to produce a ball bond on the first bond and a wedge bond on the second. Thermocompression is used on gold and in plastic packages to prevent wire sweep. Thermocompression bonds occur when two metal surfaces are brought into intimate contact through a controlled time, temperature, and pressure cycle. Typical bonding temperatures during thermocompression bonding range from 300 to 400°C. Heat is generated during the manufacturing process, either by a heated pedestal on which the assembly is placed for bonding or by a heated capillary feeding the wire. Typically, bonding time is in the neighborhood of 40 ms, which translates to a machine speed of approximately two wires per second.

Thermosonic bonding combines ultrasonic energy with the ball-bonding capillary technique of thermocompression bonding. The processes are similar, but in thermosonic bonding the capillary is not heated and substrate temperatures are maintained between 100 and 150°C. Ultrasonic bursts of energy make the bond. Typically, at the second bond, the capillary leaves a characteristic circular pattern called a *crescent bond*. The bonding time is usually about 20 ms, or a machine speed of ten wires per second, for ball bonding and three wires per second for wedge bonding.

Ultrasonic bonding is a low-temperature process in which the source of energy for the metal welding is a transducer vibrating the bonding tool parallel to the bonding pad in a frequency range from 20 to 60 kHz. Ultrasonic bonding uses aluminum wire in ceramic/metal packages. Ultrasonic processes are used for wedge-wedge bonds, for which a common centerline and careful alignment during manufacture are critical to avoid large stresses and irregular deformation. Normally, the first bond is made to the die and the second to the substrate. Referred to as *forward bonding*, this is the preferred bonding procedure because it is less susceptible to edge shorts between the die and the wire. Typical bonding time for

ultrasonic bonding is about 20 ms, which translates to a machine speed of four wires per second. A disadvantage of wedge bonding over ball bonding is the necessity of maintaining the directional first-to-second alignment by rotating and aligning the die and substrate with the direction of the wire. Rotation is difficult in large MCMs (>7 cm on the side), as most equipment was designed for much smaller integrated circuit (IC) bonding. Thus, while ultrasonic bonding has the advantage of small bond pitch, the overall speed of the process is less than that for thermosonic bonds, due to machine rotational movements.

Some quality/infant-mortality failure mechanisms associated with wirebonding include cratering of the die or chip-out due to excessive bond stress on the die. It is important to maintain adequate bonding load and temperature to allow dispersion of contaminants. Cleanliness, proper atmosphere during bonding, and surface finish are also important assembly factors. Long-term failure mechanisms include differential thermal fatigue, electrical leakage, and Kirkendall voids — voids formed by different inter-diffusion rates of gold and aluminum. Purple plague is a brittle, gold-aluminum intermetallic formed at high temperatures.

Flip Chip Bonding

Flip chip bonding is an interconnection technique in which the die is connected facedown onto the substrate. Solder bumps on area-array metallized terminals are reflowed to matching footprints of pads on a substrate. Flip chip bonding grew at a rate of about 18% compound annual growth (CAG) between 1991 and 1997. With wafer bumping services readily available, growth from now to the year 2002 is projected at nearly 50% CAG. One of the first products with extensive use of flip chip packaging was a Sony camcorder that contained sixteen flip chip die on chip-scale interposers.[9]

The three major steps involved in manufacturing flip chip bonds are (1) die or wafer bumping, (2) alignment of the die and substrate, and (3) assembly. Flip chip technology has several advantages over wirebonding:

- Self-alignment during die joining, which allows for automatic die placement and testing
- Low lead inductances, due to shorter interconnection lengths than wirebonding
- Reduced need for precious attach metals
- Increased productivity, due to the ability to make large numbers of bonds simultaneously

Evaporating and plating are the major methods of bump formation. Evaporated bumps (125 μm diameter and 100 μm high) can be smaller and more uniform than plated bumps (125–175 μm diameter and 25–100 μm high).

The flip chip assembly of a microelectronic component package is a composite of multiple, thin layers of metals. On the die bond pads, the pad structure is called *ball-limiting metallurgy* (BLM), *pad-limiting metallurgy* (PLM), or *under-bump metallurgy* (UBM). On the substrate bond pads, the connection structure is called *top-surface metallurgy* (TSM). Figure 10A1.2 shows a typical flip chip bond structure.

The BLM structure and solder bump manufacturing, called the *bumping process*, can be implemented using a variety of methods, including metal masking, photolithography, electroplating and ultrasonic soldering, maskless bumping, and copper bumping. Critical properties of the BLM adhesive layer include good electrical contact with the metallization pad on the die, strong adhesion to the pad and to the passivation layer surrounding it, and selective etchability of the metal layer, enabling the use of photolithography techniques during fabrication. The BLM barrier layer must also have good solderability and the capability to prevent interdiffusion between the solder and the pad metallization. Finally, the BLM bonding layer must provide an inert surface during bonding and protect the barrier layer from oxidation during storage.

The barrier layer of the TSM structure is made of a metal that increases wettability and has a surface suitable for solder reflow. The bonding layer uses metals that have the ability to retain wetting properties and provide adequate shelf life prior to die attachment. The melting point is the most important material property when selecting solder materials. High-melting-point solders are selected for die-level
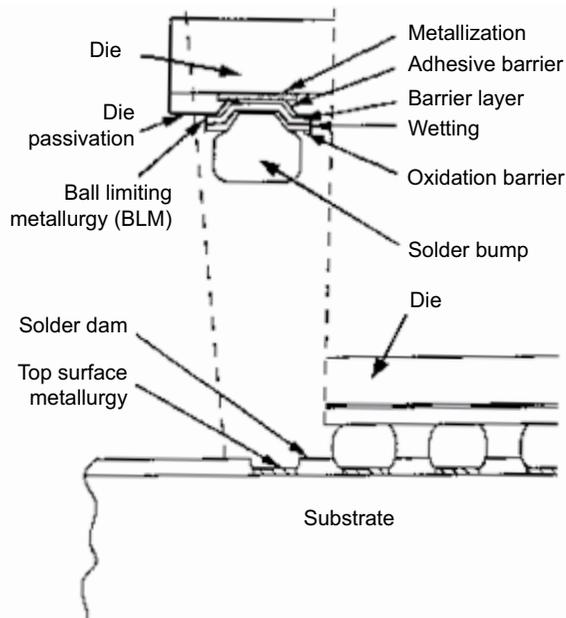
FIGURE 10A.1.2 Flip chip bond structure. (From Pecht, M. et al., *Quality Conformance and Qualification of Microelectronic Packages and Interconnects,* John Wiley & Sons, New York. With permission.)

interconnections to enable lower melting-point solders to be used for the board-level packaging. For example, 95Pb/5Sn solder (melting point around 315°C) is used with alumina ceramic substrates for die connections, while eutectic tin lead solder (melting point around 183°C) is used to attach dies to such organic substrates as Kapton film and glass/epoxy printed wiring boards.

Also important in solder selection is the cyclic strain hardening behavior of the solder, which describes the strain induced in the solder by a given stress condition. This material property strongly influences the thermal fatigue life of the solder. A slow interdiffusion rate that reduces intermetallic formation with the metal layers on the die and the substrate pads is required to enhance the thermal fatigue life of the solder. Intermetallics, though necessary to form a good bond, may reduce the thermal fatigue life if present in excessive quantities because of their brittle nature.

High corrosion resistance is required for solders used in non-hermetic packages to prevent corrosion-related failures. High oxidation resistance is also desirable, as the operational environment in non-hermetic packages accelerates solder oxidation, first on the surface and then in the bulk solder, which can eventually result in solder-die separation. High thermal conductivity is a benefit of metallic solders that allows the heat generated by the die to be dissipated to the substrate via solder bumps.

Tape-Automated Bonding (TAB)

Tape-automated bonding is particularly well suited for volume applications requiring small, lightweight, and high-I/O-count electronic packages. Furthermore, with hybrids and multichip modules, TAB has been used as a means to test and package very large-scale integration dies for a variety of products. (For TAB design guidelines and comparisons with other interconnect technologies, the interested reader is referred to Reference 2.)

The TAB assembly includes bumps, interface metallurgy, leads, lead plating, adhesive, polymeric tape, and encapsulant. In one-layer tape (all metal), the tape is made of metal foil with an etched lead pattern. In multiple-layer tape, the tape assembly consists of metal foil with an etched lead pattern and polymeric tape, with or without adhesive. A TAB assembly can be mounted onto the substrate face-up (conventional), facedown (flip-TAB), or in recessed pockets. Because of the geometry configuration, flip-TAB mounting offers options for either straight or formed leads.

TABLE 10A1.5 Dimensions of Tape-Automated Bonds[11–13]

Element of TAB	Dimensions
Bump	
Square	50–120 µm wide and 10–30 µm high
Truncated sphere	80- to 100-µm diameter and 25 µm high
Interface metallurgy	
Adhesion and barrier layers	0.08–1 µm
Bonding layer	0.1–0.3 µm
Lead	
Thickness	18–70 µm
Inner lead pitch	30–100 µm
Outer lead pitch	50–635 µm
Plating thickness	0.25–2 µm
Polymeric tape	
Width	8–70 mm
Thickness	25–127 µm
Polymeric adhesive thickness	12.7–25.4 µm
Die passivation thickness	1–1.5 µm

Common TAB dimensions are summarized in Table 10A.1.5. The bump configurations in TAB can be classified as bumped die, bumped leads (BTAB), transferred bumps (TTAB), or bumpless. The bumped-die approach requires bumping the die before bonding. One-layer tape typically consists of about 70-µm-thick etched copper foil. Two-layer tape consists of a polymeric film, approximately 50 µm thick, and a patterned metal layer of 20 to 40 µm. Three-layer tape consists of patterned metal, usually as sheets of electro-deposited or rolled copper (typically 35 µm thick), laminated with an adhesive to prepunched polymeric film (typically 125 µm thick). Two-metal-layer tapes with signal and ground planes and three-metal-layer tapes that provide signal, ground, and power planes are being used in some multichip modules.[10]

Ultrasonic bonding is typically used to create the inner-lead bond. The outer-lead bond can be ultrasonically bonded, adhesive bonded, or soldered to the board or substrate. The BTAB approach bonds an unbumped die to bumps on the tips of the inner leads. The TTAB approach bonds an unbumped die to bumps on a separate substrate, which are transferred to the inner leads. The bumpless TAB approach bonds the TAB inner leads directly to an unbumped die.

Tape-automated bonding is capable of accommodating dies with peripheral and area-array I/Os. In an area-array TAB (ATAB), a multilayer metal tape is usually used to provide interconnections between the die bumps and the substrate bonding pads. Area-array TAB increases the number of potential I/Os and improves integrated circuit design flexibility. The common inner lead pitch is 100 µm, with 50 µm wide lines and spacing.

The typical outer-lead pitch ranges from 200 to 625 µm. Tape widths can range from 8 to 70 mm to accommodate various die sizes and I/O counts. Multiple-conductor (multimetal) tapes have been developed to control impedance and reduce cross-talk.[10] An advantage of TAB is the ability to test the components at extremely fine pitches, prior to excision of the part from the tape. This practice prevents lead damage. TAB pitches of less than 50 µm are in production and perform electrically and thermally better than wirebonding.

Some disadvantages of TAB are tooling and nonrecurring costs. Each die design requires a new tape design. This reduces the flexibility to accommodate die shrinks.

Three-Dimensional Die Packaging

Three-dimensional (3-D) packaging and interconnection provide increased electrical performance and packaging density compared to traditional two-dimensional (2-D) approaches. Three-dimensional
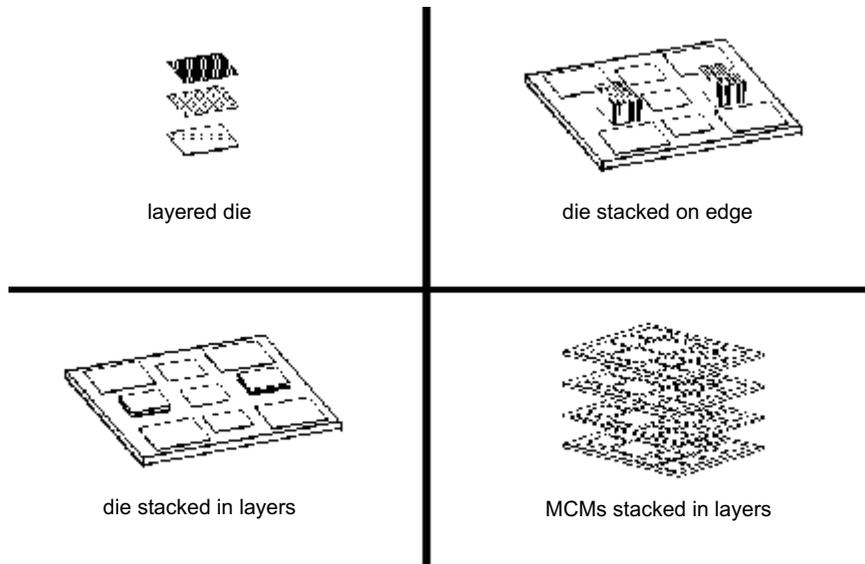
FIGURE 10A.1.3 Types of 3-D packaging. (From Pecht, M. et al., *Quality Conformance and Qualification of Micro-electronic Packages and Interconnects,* John Wiley & Sons, New York. With permission.)

packaging and interconnection can increase density by a factor of more than 50 by stacking integrated circuits (ICs). Schematically illustrated in Figure 10A1.3 are four generic types of 3-D packaging: layered dies, dies stacked on edge, dies stacked in layers, and vertically stacked multichip modules.[3]

Cost-effective multiple IC packages have been in high volume production for several years. A polyimide tape interposer is used to mount mirrored memory die. One example of this is a Sharp (Osaka, Japan) device that integrates a static RAM with a flash memory. The result not only enhances access time but also reduces the area to about half of the size of conventional packaging.[14]

Three-dimensional packaging provides increased system performance over shorter interchip connections. Also, potentially lower system power is necessary for physically smaller and fewer drivers. To reduce the package thickness and bond length, the integrated circuits are often thinned. Three-dimensional techniques incorporate many of the manufacturing processes currently used in 2-D production, adapting standard semiconductor processing equipment. Most processing is accomplished simultaneously on multiple die.

The materials used in 3-D and their critical properties are the same as those used in advanced 2-D packaging and interconnection. Common materials found in both 2-D and 3-D structures include polyimides for dielectrics, copper or aluminum for conductors, solders for bonding, and a variety of substrates using alumina, silicon, and aluminum nitride. Common properties of these materials are discussed in the literature.[1,5] Much of the success of 3-D packaging will depend on adhesive technology. Thermosetting adhesives used to bond the dies together in a stack, including polyimides and epoxies, are selected for strength and stability. Thermoplastic adhesives used to bond stacked substrates are selected for compliance and reworkability. In some cases, a hierarchy of adhesives, based on melting or softening temperature, is needed to allow disassembly of the structure; this is unique to 3-D technology.

The manufacturing process for 3-D microelectronic devices depends on the format chosen for the final product. The package elements of layered die include the die themselves, the dielectric between the die, and interconnects. The elements of dies stacked on edge, layered dies, and vertically stacked modules include dies, attachments between dies or modules, wires and wirebonds, and interconnects between dies or modules. The package-to-substrate interconnects are usually solder bumps or pad arrays.

Table 10A1.6 compares the process attributes and interconnection techniques of some of the major 3-D package manufacturers. The manufacturing yield of 3-D packages depends on the number of directly

TABLE 10A.1.6 Comparison of Three-Dimensional Packaging Technology

	Supplier					
	Texas Instrument	**Irvine Sensor**	**Irvine Sensor**	**Thomson CSF**	**General Electric**	**Hughes**
Stack approach	Edge stack	Edge stack	Layered stack	Edge or layered stack	Stacked substrate	Stacked substrate
Full IC test and burn-in	Yes	No	No	Yes	Yes	Yes
On-cube reroute required	No	Yes	Yes	No	Yes	No
Logic IC integration	Yes	No	No	No	Yes	Yes
Interconnect chip-to-chip	Epoxy w/TAB	Polyimide	Polyimide	Epoxy resin	Polymer glues	—
Interconnect of chip cube to substrate	Butt tin-lead solder joint	Flip chip solder joint	Flip chip solder joint	Wirebond	N/A	Micro-bridge technology
Chip modification	No	Yes	Yes	No	No	No
Packaging efficiency	Medium	High	High	Medium	High	High
Heat dissipation	Good	Good	Poor	Good	Poor	Poor

connected dies built into the device. For example, if the yield of a particular type of die is 90% and the completed 3-D module comprises three layers, the final yield of the module can be as low as 73%. In some format types, screening can be conducted prior to module assembly to remove defective dies from the 3-D structure or to "turn off" the defective die. In some cases, the fabrication process incorporates redundancy to minimize the number of costly screens.

In 3-D packaging, both single-level, horizontal cross-talk and cross-talk between different layers can be potential problems for very high-speed applications. Furthermore, the approach may require the use of heat spreaders when using multiple high-power devices in order to meet thermal operating specifications as well as thermal and thermomechanical stress design limits.

10A.1.2   Printed Wiring Board Technology

The printed wiring board is a substrate on which electronic components are mounted for electrical interconnection and mechanical support. The interconnection is provided by patterned metal tracks either on the surface or on the inner layers of the printed wiring board. Based on the raw materials used for manufacture, printed wiring boards can be either organic or ceramic boards. The most common organic board material consists of a woven glass fabric bound by a resin. Ceramic board materials typically include alumina, aluminum nitride, and beryllia. Often, in ceramic boards, materials and structures are added to create embedded capacitors and resistors, freeing precious top-layer real estate. While not widely in production, similar techniques can be used in the inner layers of organic boards.

Conventional Printed Circuit Board Technology

Conventional printed wiring board (PWB) technology can be categorized as single layer, double layer, or multilayer. Single-layer boards have conductors etched on one side of the board, usually without hole plating. Double-layer boards have conductors on both sides of the board, but no inner layers. Multilayer organic boards typically consist of stacks of partially or fully cured fabric-reinforced epoxy sheets and copper foil conductors.

While there are many ways to fabricate a multilayer printed wiring board, a typical flow chart of the fabrication process is shown in Figure 10A.1.4.[1] In conventional printed circuit board technology, the

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┌─────────────────┐              ┌─────────────────┐
│ Printed circuit │              │ Printed circuit │
│ laminate material│             │ laminate material│
└────────┬────────┘              └────────┬────────┘
         │                                │
         ▼                                ▼
┌─────────────────┐              ┌─────────────────┐
│    Sheared      │              │ Dry-film image  │
│  into panels    │              │  for etching    │
└────────┬────────┘              └────────┬────────┘
         │                                │
         ▼                                ▼
┌─────────────────┐              ┌─────────────────┐
│  Tooling holes  │              │   Etch copper   │
│ drilled or pierced│            └────────┬────────┘
└────────┬────────┘                       │
         │                                ▼
         ▼                       ┌─────────────────┐
┌─────────────────┐◄──────┐      │   Resist strip  │
│  Circuit holes  │       │      └────────┬────────┘
│ drilled or pierced│     │               │
└────────┬────────┘       │               ▼
         │                │      ┌─────────────────┐
         ▼                │      │   Black oxide   │
┌─────────────────┐       │      └────────┬────────┘
│   Deburring     │       │               │
│   of holes      │       │               ▼
└────────┬────────┘       │      ┌─────────────────┐
         │                │      │   Cut prepreg   │
         ▼                │      └────────┬────────┘
┌─────────────────┐       │               │
│   Electroless   │       │               ▼
│  copper plate   │       │      ┌─────────────────┐
└────────┬────────┘       │      │   Inner layer/  │
         │                │      │ prepreg booking │
         ▼                │      └────────┬────────┘
┌─────────────────┐       │               │
│ Dry-film/screen │       │               ▼
│ image for plating│      │      ┌─────────────────┐
└────────┬────────┘       │      │    Press into   │
         │                └──────│ multilayer panels│
         ▼                       └─────────────────┘
┌─────────────────┐
│  Pattern plate  │
└────────┬────────┘
         │
         ▼
┌─────────────────┐
│ Resist strip/etch│
└────────┬────────┘
         │
         ▼
┌─────────────────┐
│    Contact      │
│ finger plating  │
└────────┬────────┘
         │
         ▼
┌─────────────────┐
│     Reflow      │
└────────┬────────┘
         │
         ▼
┌─────────────────┐
│   Inspection    │
└────────┬────────┘
         │
         ▼
┌─────────────────┐
│   Solder mask   │
└─────────────────┘
```
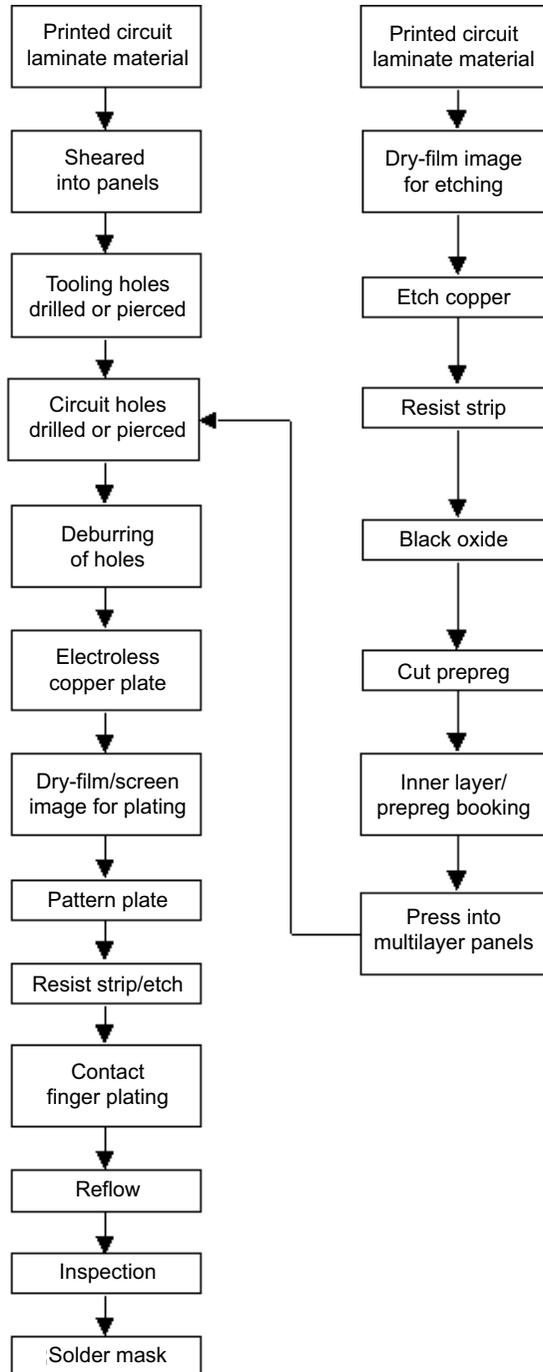
FIGURE 10A.1.4 Typical multilayer PWB fabrication process.

conductors are generally formed through both subtractive and additive processes. The partially cured laminate sheets, called *prepreg*, are cured and laminated with pressure and temperature.

The most common and least expensive resin system is FR-4 epoxy. This epoxy is a diglycidyl ether of tetrabromobisphenol A, with a glass transition temperature ranging from 135 to 180°C. Variations are

TABLE 10A.1.7 Comparison of Common Printed Wiring Board Materials

Substrate Material	Glass Transition Temp. (°C)	Dielectric Constant @ 1 MHz	Dissipation Factor @ 1 MHz	In-Plane CTE (ppm/K)	Relative Cost (FR-4 = 1)
FR-4 epoxy-glass	125–135	4.10–4.60	0.028–0.030	14–16	1
Polyfunctional FR-4	140–150	4.10–4.60	0.028–0.030	14–16	1.1–1.5
Multifunctional FR-4	150–170	4.10–4.60	0.028–0.030	14–16	1.1–1.5
Polyimide-glass	210–220	3.95–4.05	0.01–0.015	12–14	2–3
BT epoxy	180–190	3.85–4.10	0.011–0.013	13–17	1.1–1.5
Cyanate ester-glass	240–250	3.50–3.60	0.005–0.007	11–15	4–5
PPO epoxy	175–185	3.80–4.20	0.008–0.009	12–13	2–3
PTFE-glass	327 melting	2.45–2.55	0.001–0.003	70–120	15
Alumina	N/A	8.90	.0002–.0015	6.8	8–12

sometimes introduced in the resin to tailor desirable mechanical and electrical properties, including glass transition temperature, dielectric constant, coefficient of thermal expansion, moisture absorption, and thermal conductivity.

Holes in conventional PWBs are typically mechanically drilled. Those holes that allow conduction through all layers are called *plated through-holes* (PTH) for through-hole leads. For surface-mount devices, the holes are referred to as *plated through-vias* (PTV). Blind vias begin at a surface layer of the board and end at an internal layer. Buried vias are located in internal layers and do not include the external layers.

The explosion of commercial wireless (1–2 GHz) and high-performance processors (>1 GHz) is challenging the limits of FR-4. The edge rates of the signals and clock are actually more critical to application design than the clock frequency. The dissipation factor correlates with signal distortion and the dielectric constant with the signal delay. Thus, the relatively high dielectric constant of FR-4 (4.2) and high dissipation factor (0.030) make FR-4 use increasingly difficult for high-frequency (>150-MHz board frequencies) and fast-edge-rate (less than 1–2 ns) applications. While polytetrafluoroethylene (PTFE) materials have been used in military and high-end commercial applications for three decades because of their low dielectric constant of 2.4 to 2.6, these materials tend to be about 15 times costlier than FR-4. New materials such as polyphenylene oxide (PPO)/epoxy have reduced the dissipation factor significantly. Higher performance resins, such as polyfunctional FR-4 epoxy, bismaleimide triazine/epoxy (BT), cyanate esters (CE), and polyimide, are also used for a variety of special applications. Some key parameters and the relative costs of common materials are summarized in Table 10A.1.7.

Printed wiring boards can also be connected by flexible dielectric materials called flex print. The rigid portion of printed wiring boards can be either organic or ceramic, while flexible circuits use thinner, flexible organic base materials, including polyester and polyimide. Flex print provides an interconnection between boards that can be electrically superior to conventional connectors.

High-Density Interconnect Technology

Driven by increasing component I/O densities, board technology is migrating to the high-density interconnection (HDI). While there are numerous processes to form HDI layers, these can be classified into two general categories: microvia and thin-film. The microvia approach offers many advantages, including high frequency, high clock-rate performance, high wiring densities, and high ratios of active device area to substrate area. While the increased density comes at a higher cost, the per-function cost can actually be significantly lower. Thin-film HDI technology has been used in space applications and supercomputer applications.
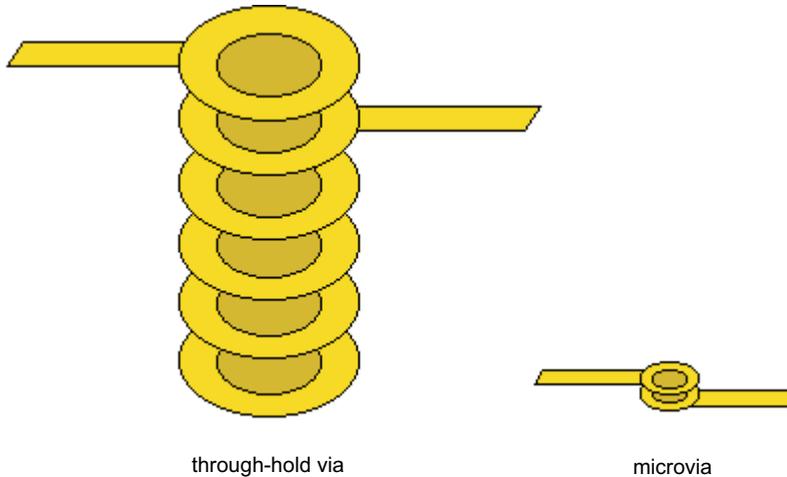
through-hold via   microvia

FIGURE 10A.1.5 Size advantage of microvia technology. (From IPC, *HDI and Microvia Technology,* Institute for Interconnecting and Packaging Electronic Circuits, Northbrook, IL, www.ipc.org/html/hdi.htm. With permission.)

Microvia HDI

Microvia HDI is becoming increasingly important with the advent of fine pitch array packaging. The Institute for Interconnecting and Packaging Electronic Circuits (IPC) defines a microvia as a blind or buried via of less than 150 μm, with a capture pad of less than 300 μm. Microvias can be used with conventional boards or chip-level packaging. In conventional boards, microvia technologies can be used selectively to redistribute difficult-to-route areas and enable components on both sides of the board. Ball grid arrays (BGAs) and CSPs with pitches of less than 1 mm typically require microvia redistribution layers. Figure 10A.1.5 shows the size advantage of microvias over conventional multilayer plated through-vias. Figure 10A.1.6 is a typical microvia stack-up; note that the microvia is actually included in the component solder pad. Current volume production yields exceed 99% in Japan and Taiwan. The microvias are generally formed by three basic approaches: plasma etch, photoimaging, and laser ablation. Laser ablation is a sequential technique, while plasma etch and photoimaging form vias simultaneously. Due to the high energy and difficulty of ablating glass fiber, the materials are typically not reinforced. Mechanical drilling can also be cost effective in material from 250 μm thick down to about 125 μm thick.[15]

Because there is no glass reinforcement, the dielectric constant of FR-4 epoxy is significantly lower than its reinforced counterpart. DYCOstrate®, developed by Dyconex of Zurich, Switzerland, is widely used in East Asia. An isotropic oxygen plasma is used to form vias that range from 75 to 150 μm in diameter. One advantage of this process is that the plasma removes all organic material, leaving the microvia clean.[17] The parallel processing and high yield make this process very cost effective.

A liquid- or dry-film photoimageable dielectric is generally an epoxy-acrylate material. Processing is similar to conventional soldermasking, followed by copper plating and patterning. Via diameters range from 50 to 250 μm.

Both CO_2 and ultraviolet (UV) lasers can be used to ablate the dielectric; UV can also burn through the copper layers. The CO_2 lasers are able to produce much smaller holes (10–25 μm) and are faster than the UV laser (25–200 μm). Laser vias can be formed in a variety of ways, including a two-pass process (first through copper, followed by a dielectric at a different frequency), a combination of conventional etching through the copper and laser ablation of the dielectric, and, finally, a deposited dielectric with laser via formation followed by an additive outer copper layer.[18] The remaining residue at the bottom of the ablated via can be removed with potassium permanganate or plasma etching for higher aspect ratio holes.
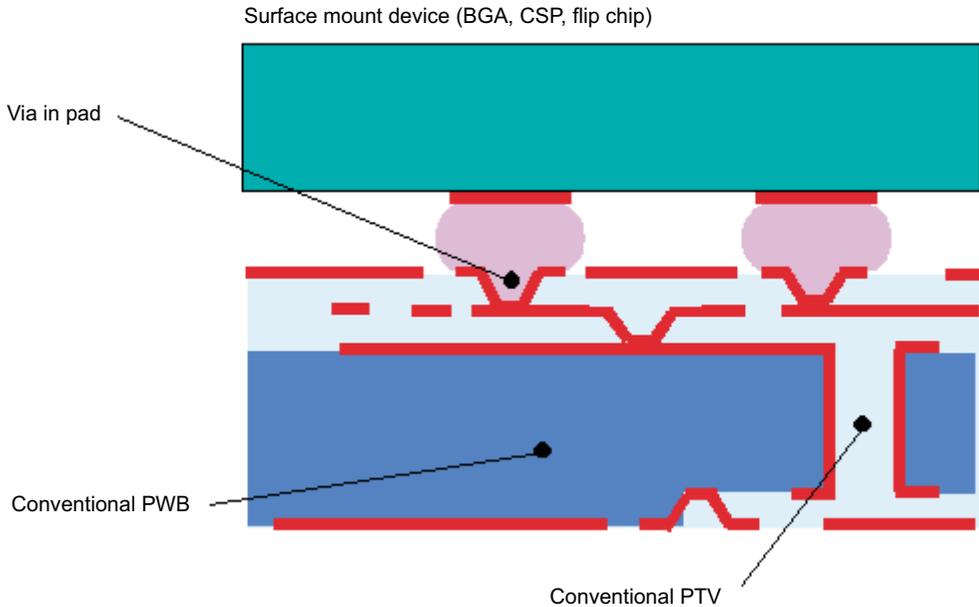
Surface mount device (BGA, CSP, flip chip)

Via in pad

Conventional PWB

Conventional PTV

FIGURE 10A.1.6 Example of microvia technology. (From IPC, *HDI and Microvia Technology,* Institute for Interconnecting and Packaging Electronic Circuits, Northbrook, IL, www.ipc.org/html/hdi.htm. With permission.)

The reliability of the microvias is generally excellent, due to an aspect ratio of less than one. Other critical reliability factors are the hole diameter, plating thickness, hole cleanliness, and plating uniformity. In a sample of 15 different microvia test cases, only two test cases could not pass 2000 liquid-to-liquid thermal shock cycles (–55 to 125°C).[19] In another study of 18 U.S. and European fabricators, strong correlation was found between hole diameter and reliability. Holes of less than 150 μm were not reliable. Vias in solder pads were found to have no impact on solder-joint reliability.

Thin-Film HDI

All thin-film HDI approaches use deposited thin-film conductors with organic or inorganic interlayer dielectrics. The materials are sputtered with processes similar to semiconductor processing. Vias provide interconnection between conductor layers. Fully assembled modules using thin-film HDI are referred to as MCM-Ds.

Thin-film HDI can be classified into four generic types: overlay HDI, reach-through via HDI, beveled die-edge HDI, and conventional, chip-last, MCM-D, thin-film conductor and deposited dielectric HDI. A chip-last approach may employ wirebonding or other interconnects for die-to-substrate connectivity.

Table 10A.1.8 illustrates some of the many manufacturers and research institutions that make various types of HDI and MCM-D substrates. Typical design considerations, such as the number of metal layers, conductor line width, line spacing, via diameter, and via pitch, are listed in Table 10A.1.8 for each manufacturer. While many layers of dielectric and metal are possible, applications are often easily routed in two signal layers and a power-and-ground layer.

Ceramic Substrate Technology

Thick-film ceramic boards are formed by screen printing conductive, resistive, and dielectric paste onto a dielectric substrate and then firing. Typical thicknesses are in the range of 10 to 60 μm, depending on the materials. The classification "thin-film" refers to materials that are deposited in a sputtered vacuum process, similar to that used in semiconductor fabrication. Thin-film feature sizes are an order of

TABLE 10A.1.8 HDI and MCM-D Capabilities

Manufacturer	Maximum Number of Metal Layers	Minimum Line Width (μm)	Minimum Via Diameter (μm)	Minimum Line Spacing (μm)	Minimum Via Pitch (μm)
Rogers Corp.	9	50	75	125	150
AT&T	4	50	150	120	200
Toshiba	8	40	50	114	150
MMS	11	18	25	75	75
NEC	8	25	50	75	75
NTK	6	25	25	63	63
Hughes	10	15	20	60	60
Narumi	4	10	20	60	60
Kyocera	7	25	50	50	50
GE	5	37	44	50	114
HP	7	15	6	30	30
MCC	8	8	8	25	25
NChip	5	10	8	25	25
Midway	8	10	10	20	20
NTT	4	3	15	20	25
Polycon	8	5	5	10	10

magnitude less than the thick-film structures. These hybrid composites can have multiple conductor layers and can include both thick- and thin-film processes.

10A.1.3 Printed Circuit Assembly Processes

The printed circuit assembly processes consist of placing components on the printed wiring board, soldering the components, and post-solder processing steps such as cleaning and conformal coating. Classification of soldering processes is based on the method of applying the solder and the heating processes involved. Two processes in common use are wave soldering and reflow soldering. Wave soldering is used primarily for through-hole technology, while reflow soldering is used for surface-mount assembly.

Through-Hole Assembly

Through-hole components can be placed manually or with automated insertion equipment. High-speed equipment can place more than a thousand devices per minute, crimp the leads on the opposite side of the board, and dress the lead to an appropriate length. In wave soldering, the board is passed over a jet of molten solder. The hydrostatic pressure of the solder from the nozzle wets the underside of the PWB and pushes the solder slightly up the plated through-hole. Subsequent capillary action, resulting from the surface tension between the solder and the walls of the plated through-hole, forces the molten solder to rise through the hole and wet the upper lands of the through-hole, securing the part in place.

  Before soldering, boards must be fluxed and preheated. Fluxing consists of applying a chemical compound with activators, solvents, and detergents to the solder-joint locations to chemically clean the surfaces to be joined. Preheating reduces thermal shock to the components and the PWB, activates the flux, and evaporates any flux solvents to prevent the formation of blowholes (voids) in the solder joint.

SMT Assembly

The reflow soldering process consists of remelting solder previously applied to a PWB joint site (pad) in the form of a preform or paste. No solder is added during reflow. The first step in the process is to apply solder paste and any necessary adhesives to the land patterns on the printed wiring board. Adhesives are needed only if the components cannot be held in place by the tackiness of the solder paste. After

component placement, the populated PWB is transported to the preheater to evaporate solvents in the solder paste. In this stage, the temperature of the board is raised to 100 to 150°C at a rate low enough to prevent solvent boiling and the formation of solder balls; 2°C/second has been accepted as an industry norm.[20]

The next stage in the reflow process is slow heating, which increases the temperature to the solder melting point and activates the flux in the solder paste. The activated flux removes oxides and contaminants from the surfaces of the metals to be joined. The next stage consists of melting the solder. During the melting stage, the temperature of the solder paste is raised to just above its melting point. When the solder melts, it replaces the liquid flux formed in the previous step. The temperature is held above the melting point while the solder coats the surfaces to be joined. The temperature must be regulated to allow the melted solder particles to coalesce and form a fillet around the component lead. Excessive temperatures increase the fluidity of the solder, causing it to move away from the desired joint location, while excessively long periods at the wetting temperature may lead to intermetallic formation and embrittlement. Fillet formation is the most critical part of the reflow process. The last stage involves cooling the solder joint, either by conducting the heat through the board layers or by natural or forced convection to the ambient air.

Reflow methods differ according to the method of heat transfer to the reflow site. Conductive, convective, and radiative heat transfers are variously used for this purpose. Conductive heat-transfer methods include the soldering iron, hot-bar reflow, and conductive-belt reflow. Radiative heat-transfer methodologies include infrared, laser, and optical fiber systems. Convective heat transfer is used in vapor-phase (or condensation) reflow systems. Each method has its own merits and limitations. The most common technique for mass reflow soldering is infrared heating/convection because it allows temperature control throughout the reflow soldering cycle. However, vapor-phase soldering is still considered the best way to limit the maximum temperature reached during reflow, as the temperature in the oven never rises above the temperature of the saturated vapor.

Connectors

Connectors can be classified based on the electronic elements being connected. Board-to-board connectors are used to connect two printed circuit boards; wire-to-board connectors are usually used to connect a source of power to a printed circuit board or to bus signals with high fidelity; and wire-to-wire connectors are generally used externally to the electronic equipment. In contemporary systems, connectors are a vital link in completing an electronic system. Connectors should be chosen carefully, taking into consideration current, voltage, impedance, EMI/EMR shielding, and allowable losses.

A connector is composed of four basic elements:[21] the contact interface, the contact finish, the contact spring, and the connector housing. The contact interfaces are of two kinds: separable and permanent. The separable connector allows for mating and unmating, while the permanent interface does not. The contact finish aids in establishing a contact interface and protecting the contact springs from corrosion. The contact spring is the electrically conducting element between the permanent connection to the subsystems and the separable interface that supplies the force necessary to maintain contact at the separable interface. The connector housing performs both mechanical and electrical functions by electrically insulating the individual contacts and supporting and locating them mechanically.

Board-to-board connectors are an important part of today's packaging. Commercial applications are making high-density connectors inexpensive. Mezzanine assemblies are gaining popularity, as processor modules become more complex in order to accommodate processor upgrades. One example is Intel's Pentium II® Mobile Module, which uses a 400-pin, 1.27-mm pitch connector.[22]

10A.1.4   Electronic Packaging Future

The future of electronic packaging promises an accelerating change. For several years now, industry roadmaps have assessed the capabilities, needs, direction, and future of electronic packaging. Hundreds

of companies, government agencies, consortia, and universities have contributed to roadmaps. There are a number of these long-range plans, including the National Electronics Manufacturing Initiative (NEMI),[14] the Japan Printed Circuit Association's *Report on the Technology Roadmap for Advanced System Integration and Packaging*,[23] and IPC's *The National Technology Roadmap for Electronic Interconnections*.[24] Many large companies and research universities involved in packaging, such as the University of Maryland's CALCE Electronic Products and Systems Center, also have roadmaps that complement and fill research holes.

The most recent findings are that cost is king in nearly all applications. Cost, a major driver in the advancement of technology, is also driving the trend toward electronics manufacturing service (EMS) suppliers or contract manufacturers. Cost and business pressures are fueling the 25% annual increase in EMS providers. The advantages of EMS include optimizing manufacturing cycle times, reducing working capital, and improving quality. The NEMI roadmap suggests that a downside of this EMS trend will be a slowing of research and development, as the EMS providers will push to keep the *status quo* rather than advance to less proven areas. The NEMI roadmap predicts that this will also lead to shorter product cycles and more conservative, evolutionary packaging approaches. If the new technology cannot achieve cost parity with existing technologies, then industry acceptance will be delayed. One example of this is flip chip packaging, competing with those technologies that are now widely used: CSP and BGA.[25]

The NEMI, IPC, and the Semiconductor Industry Association roadmaps all predict a movement from peripheral to array packaging; consequently, peripheral packages will not decrease below a 0.5-mm pitch. The growth of flip chip interconnection was seen as a growing trend in the industry by all roadmaps. The NEMI roadmap sees integral passives (resistors and capacitors) as an important part of the future in portable electronics, whereas the IPC sees the enabling technologies as immature.[26]

Some recent predictions from the NEMI roadmap are summarized in Tables 10A.1.9 and 10A.1.10. The cost of I/O and labor to assemble packages will continue to fall dramatically. Substrate lines, spaces, and device I/O pitch will also shrink to keep pace with silicon integration. Noncontact test infrastructure

TABLE 10A.1.9 NEMI Predictions for the Future[25]

	1999	2003
IC package costs per I/O (¢)	0.7–0.9	0.4–0.6
Board assembly conversion (¢)	0.7–0.9	0.5
Substrate lines and spaces (μm)	70	35
Process test pads (mm)	0.5	Non-contact
Flip chip pad pitch (μm)	180	130

TABLE 10A.1.10 Package Forecast by Lead Count Range

I/O	1998	2003
4–18	28,495	38,768
20–32	16,347	20,489
36–68	8442	18,502
72–100	2043	5160
104–144	1551	3222
148–208	922	2378
212–304	405	1070
308+	511	1710
Total	58,716	91,299

From Berry, S., The future of leadcounts, *HDI,* 2(4), 14–16, 1999. With permission.

will be required to provide efficient and cost effective assurance that assemblies are functional. A shift to higher pin-count packages is also expected, as shown in Table 10A.1.10. While the current percentage of packages with a pin count greater than 304 is less than 1%, the percentage in the year 2003 will nearly double.

Electronic packaging technology will continue to enable many compact and high-speed products of the 21st century. The need for innovations in cost, yields, and productivity will certainly challenge those engineers involved in the many facets of packaging. These improvements will eventually touch and, it is hoped, enhance the quality of life of all the world's people.

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